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Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF ENGLISH TRANSLATIONS

Sir:

Referencing the amendment dated October 27, 2002 in the above-identified application, English translations of Japanese document No. 1996-358954 filed December 10, 1996 and Japanese document No. 1996-358955 filed December 30, 1996 are filed herewith to perfect the Japanese priority date.

Verification of the translations dated October 18, 2002 are also enclosed.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

November 4, 2002
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Signature

Susan Regan
Typed or Printed Name of Person Signing Certificate

Acknowledgement of the enclosures and consideration with confirmation are earnestly solicited.

Respectfully submitted,

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In re U. S. Patent Application)
Serial No.: 09/455991)
Filed: December 6, 1996)
For: SEMICONDUCTOR DEVICE AND)
METHOD OF MANUFACTURING THE SAME)

VERIFICATION OF TRANSLATION

Sir:

I, Etsuko FUJIMOTO, 303 Charm KY, Higashi-Fuchinobe, Sagamihara-shi, Kanagawa-ken 229-0005 Japan, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and that to the best of my knowledge and belief the following is a true and correct translation of the above referenced Japan Patent Application No. 1996-358954 filed on December 30, 1996.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements.

Date: this 18 day of October, 2002

Etsuko F.

Name: Etsuko FUJIMOTO

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[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] SEMICONDUCTOR CIRCUIT

[Claims]

[Claim 1]

1. A semiconductor circuit, comprising:

a circuit having at least one thin-film transistor formed on an insulating substrate;

wherein an active layer of said thin-film transistor is constituted by using a region where crystal grows in parallel to a substrate from a metal element added region to which metal elements that promote crystallization of silicon having a longitudinal shape are added;

wherein a longitudinal direction of the metal element added region is identical or substantially identical with a direction of moving carriers in the active layer; and

wherein the metal element added region extends longer over an end portion of the active layer.

[Claim 2]

A semiconductor circuit according to claim 1,

wherein a distance by which the metal element added region extends longer from an end portion of the active layer is set to 50% or more of the crystal growth distance.

[Claim 3]

A semiconductor circuit according to claim 1,

wherein the active layer is disposed within a region where the metal elements are linearly diffused from the metal element added region during a crystallizing process.

[Claim 4]

A semiconductor circuit according to claim 1,

wherein a direction of moving carriers in an island region of semiconductor which constitutes a thin-film transistor is substantially identical with a direction of the continuity of a crystal structure.

[Claim 5]

A semiconductor circuit according to claim 1,

wherein the metal elements consist of one or plural kinds

of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

[Claim 6]

A method of manufacturing a semiconductor circuit, comprising the steps of:

forming an amorphous silicon film on a substrate having an insulating surface;

forming a metal element added region where metal elements that promote the crystallization of silicon which is longitudinally shaped is added on said amorphous silicon film; and

conducting a heat treatment to allow crystal to grow in parallel to said substrate from said metal element added region;

wherein said metal element added region extends longitudinally over an end portion of a semiconductor active layer pattern which will be formed in a post-process by a predetermined distance.

[Claim 7]

A method of manufacturing a semiconductor circuit according to claim 6,

wherein a distance by which the metal element added region extends longer from an end portion of the active layer is set to 50% or more of the crystal growth distance.

[Claim 8]

A method of manufacturing a semiconductor circuit according to claim 6,

wherein the metal elements consist of one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to a thin-film transistor circuit and a liquid-crystal display using a thin-film transistor. In particular, the present invention relates to

a method of manufacturing a thin-film transistor circuit on an insulation substrate made of glass, quartz or the like, or in an SOI where an insulation layer is disposed on a mono-crystal.

[0002]

[DESCRIPTION OF THE PRIOR ART]

There has been known a technique in which a silicon film having crystallinity is formed on a glass substrate or a quartz substrate, and a thin-film transistor is manufactured using the silicon film.

At present, the integration of a peripheral drive circuit where a drive circuit consisting of TFTs for a liquid-crystal display device is integrally formed in a periphery of a pixel matrix on a substrate instead of an LSI has been developed.

The integration of the drive circuit enables the liquid-crystal display device to be downsized and the costs to be reduced.

In such a construction, the higher speed operation of the peripheral drive circuit has been required.

However, it is difficult to obtain a required high-speed operation in the existing circuit which has been formed using high-temperature polysilicon TFTs or low-temperature polysilicon TFTs.

[0003]

It has been found that required high-speed drive is obtained by addition of a process for adding metal elements that promote the crystallinity of an amorphous semiconductor layer.

However, the individual thin-film transistors obtained through the above process still suffer from such a problem that their drive speed and electric characteristic are ununiform, etc.

[0004]

[PURPOSE TO BE SOLVED BY THE INVENTION]

The present invention has been aimed to provide a method of manufacturing a thin-film transistor circuit that requires the above-mentioned high-speed operation (in general, the

operation speed of several tens MHz or more).

[0005]

Up to now, because the metal elements that promote crystallinity are impurities for the thin-film transistors, and cannot be completely removed even though they are removed during a process after crystallization, it has been considered that the addition of the metal elements with the minimum amount as required is desirable.

Under the above circumstances, a metal element added region 105 formed for promoting the crystallinity is so shaped as to be identical with or smaller than a semiconductor island region 101 as shown in Fig. 1(b).

[0006]

The metal elements as added are diffused in the form of an ellipse through a heating process as shown in Fig. 1(b), to promote the crystallization of a semiconductor region.

However, the semiconductor island region 101 which has been crystallized in the conventional method as shown in Fig. 1(b) has a semiconductor region 101 existing in a metal element diffusion region. A variation in the characteristics of the respective transistors has been found although crystallization is promoted.

[0007]

The present inventors have investigated a cause of the variation in the characteristics of the transistors. As a result, the present inventors have proved that a direction along which crystal of the semiconductor island region 101 grows is not identical with a direction along which carriers move in the semiconductor island region that constitutes a thin-film transistor as it is apart from a metal element added region 105.

[0008]

[METHOD TO SOLVE THE PURPOSE]

In order to solve the above object, according to one aspect of the present invention, there is provided a semiconductor circuit which comprises:

a circuit having at least one thin-film transistor formed on an insulating substrate;

wherein an active layer of said thin-film transistor is constituted by using a region where crystal grows in parallel to a substrate from a region to which metal elements that promote crystallization of silicon having a longitudinal shape are added;

wherein a longitudinal direction of the region to which the metal elements are added is identical or nearly identical with a direction of moving carriers in the active layer; and

wherein the region to which the metal elements are added extends longer over an end portion of the active layer.

[0009]

In the above construction, it is important that the active layer is disposed within a region where the metal elements are linearly diffused from the region to which the metal elements are added during a crystallizing process. In other words, it is important to form the active layer utilizing not a region where crystal grows radially (that is, two-dimensionally) as shown in Fig. 1(b) but a region where crystal growth is uniformly and linearly directed to one orientation in parallel as shown in Fig. 1(a).

[0010]

The metal elements that promote the crystallization of silicon may consist of one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

[0011]

Also, according to another aspect of the present invention, there is provided a method of manufacturing a semiconductor circuit, said method comprising the steps of:

forming an amorphous silicon film on a substrate having an insulating surface;

forming a metal element added region where metal elements that promote the crystallization of silicon which is longitudinally shaped is added on said amorphous silicon film; and

conducting a heat treatment to allow crystal to grow in parallel to said substrate from said metal element added region;

wherein said metal element added region extends longitudinally over an end portion of a semiconductor active layer pattern which will be formed in a post-process by a predetermined distance.

[0012]

In the present invention, there is provided a metal element added region 105 as shown in Fig. 1(a). Reference numeral 101 denotes a semiconductor region; 102, a source line; 103, a gate line; and 104, a drain line.

[0013]

In other words,

in a circuit having at least one thin-film transistor formed on an insulating substrate,

the metal element added region 105 is disposed apart from a semiconductor island region 101 that forms said thin-film transistor by a distance y,

has a width w, and

extends longitudinally over an end portion of the semiconductor island region 101 by a distance x.

[0014]

According to the present invention, during a process of selectively introducing the metal elements that promote the crystallization of silicon into a part of the amorphous silicon film, the metal element added region 105 formed using a mask having an opening portion is disposed apart from the semiconductor island region 101 by the distance y, has the width w and is shaped to be longer toward a longitudinal direction thereof over the end portion of the semiconductor island region 101 by the distance x.

[0015]

It is desirable that the distance x by which the metal element added region 105 extends longitudinally from the end portion of the semiconductor island region 101 in the present invention is set to at least 100 μm or more.

However, in the case where it cannot be set to 100 μm or more from the viewpoint of the circuit wiring, the distance x may be set within the possible limits.

[0016]

It is desirable that the distance y between the semiconductor island region 101 and the metal element added region 105 is set to 10 μm or more. However, in the case where it cannot be set to 10 μm or more from the viewpoint of the circuit wiring, the distance y may be set within the possible limits.

Also, it is desirable that the width w of the metal element added region 105 is set to about 10 to 20 μm.

[0017]

With the above structure, the metal elements diffuse as indicated in Fig. 2(a), and promote the crystallization of the amorphous silicon film during a amorphous silicon film crystallizing process after the formation of the metal element added region.

[0018]

With the above structure, the entire silicon film whose crystallization has been promoted has a crystal structure having a continuous and linear crystal grains in a direction indicated by an arrow in Fig. 2(a).

Also, as shown in Fig. 2(b) which is a cross-sectional view taken along a line b-b' of Fig. 2(a), crystal growth progresses in parallel to the substrate.

[0019]

The crystal growth progresses from the metal element added region 405 toward the periphery thereof linearly toward the direction indicated by the arrows. According to the present invention, a region where the crystal growth progresses linearly is broadened in such a manner that the crystal grains in the entire semiconductor island region are directed to the same orientations with respect to the metal element added region.

The crystal growth in parallel to the substrate is called

"lateral growth".

[0020]

Then, it is desirable that the metal element added region 105 is disposed so that the semiconductor island region 101 is disposed within the region where the metal elements linearly diffuse.

[0021]

Also, if the distance x is set to 50% or more of the crystal growth distance, the region where the semiconductor island region 101 is formed can be made the region where the crystal growth linearly progresses.

[0022]

Also, a higher-speed operation can be expected if a direction of moving the carriers in the semiconductor island region 101 that constitutes the thin-film transistor (a carrier moving direction as a whole) is substantially identical with a direction of the continuity of the crystal structure.

[0023]

It should be noted that in the case where a plurality of thin-film transistors are continuously disposed in series or in parallel, a metal element added region having a width w may be provided which extends longitudinally from an end portion of the semiconductor island region of the thin-film transistor which is situated at its endmost by an interval y and a distance x.

[0024]

The metal element added region according to the present invention is removed through a process of removing the metal elements after crystallization.

However, because metal elements are added to a portion close to the opening portion so as to be liable to be etched, a shape mark of the metal element added region remains by over-etched as shown in Fig. 3(C).

[0025]

It is presumed that a larger amount of metal elements for promoting crystallinity remain in the vicinity of the mark

having a shape of the opening portion in comparison with other places. If wiring is formed on the mark after removal of the metal elements, diffusion caused by the process after the removal of the metal elements can be prevented.

[0026]

As one method of obtaining the crystalline silicon film according to the present invention, the following method is recommended. That is, metal elements that promote the crystallization of silicon which is represented by nickel are introduced into an amorphous silicon film, a heat treatment is then conducted on the amorphous silicon film, and thereafter a heat treatment is conducted on the film under an atmosphere containing halogen elements therein, to thereby obtain a crystalline silicon film.

[0027]

The most preferable one of the above metal elements is nickel from the viewpoints of reproducibility and advantages. In general, the metal elements of this type can consist of one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

[0028]

In the case of employing the nickel elements, the concentration of nickel that finally remains in a silicon film is about 1×10^{14} atoms/cm^3 to 5×10^{18} atoms/cm^3 in the existing circumstances, but more preferable as it is low. Researching the best conditions of gettering during the formation of a thermal oxide film, the upper limit of the concentration can be reduced up to about 5×10^{17} atoms/cm^3. The measurement of the concentration can be performed employing an SIMS (secondary ion mass spectroscopy).

[0029]

In general, the lower limit of the above concentration of nickel is about 1×10^{16} atoms/cm^3. This is because it is normally difficult to remove the influence of nickel which is attached to the substrate or the device from the viewpoint of the costs.

[0030]

Hence, in the normal manufacturing process, the concentration of remaining nickel elements is 1×10^{16} atoms/cm^3 to 5×10^{17} atoms/cm^3.

[0031]

Also, during a process of manufacturing a thermal oxide film, the distribution of the concentration of nickel elements in a thickwise direction of the crystalline silicon film as obtained is sloped or distributed because the metal elements move in the thermal oxide film.

[0032]

In general, it has been observed that the concentration of the metal elements in the crystalline silicon film tends to be heightened toward an interface where the thermal oxide film is formed. Also, it has been observed that the concentration of the metal elements tends to be heightened toward a substrate or an underlayer, that is, toward an interface of a reverse side of the thermal oxide film depending on conditions.

[0033]

Further, in the case where halogen elements are contained in the atmosphere at the time of forming the thermal oxide film, the halogen elements also exhibit the same concentration distribution as that of the above metal element. That is, the distribution of the concentration exhibits such that the concentration of the contents is heightened toward a front surface and/or a rear surface of the crystalline silicon film.

[0034]

The crystalline silicon film according to the present invention is set preferably to 100 Å to 750 Å, more preferably to 150 Å to 450 Å in final thickness. With this thickness, the singular crystal structure where crystallinity is linearly continuous can be obtained with an excellent reproducibility and with a more remarkable form.

[0035]

The final thickness of the crystalline silicon film need to be determined taking into consideration that the thickness is reduced by formation of the thermal oxide film.

[0036]

As a method of introducing the metal element, there are a method of coating a solvent containing the metal elements, a method using a CVD method, a method using a sputtering method or a vapor deposition method, a method conducting a plasma processing using an electrode containing the metal, and a method using a gas adsorbing method.

[0037]

As a method of introducing the halogen elements, there can be used means for allowing HCl, HF, HBr, Cl_2, F_2, Br_2, CF_4 and so on to be contained in an oxidizing atmosphere (for example, oxygen atmosphere).

[0038]

It is also effective that hydrogen gas is additionally introduced in the atmosphere at the time of forming the thermal oxide film to employ the action of wet oxidation.

[0039]

A temperature at which the thermal oxide film is formed is very important. In the case of obtaining a TFT that can conduct the operation of several tens MHz or more by a single element and has an S value of 100 (mV/dec) or less, a heating temperature at the time of forming the thermal oxide film need to be set to preferably 800 ℃ or more, more preferably 900 ℃ or more.

[0040]

The upper limit of the heating temperature is properly set to about 1,100 ℃ which is the upper limit of the heat-resistant temperature of a quartz substrate.

[0041]

[PREFERRED EMBODIMENTS]

[First Embodiment]

Fig. 3(A) shows a case in which a switch circuit made

up of thin-film transistors is applied to a drive circuit of a liquid-crystal display device in accordance with one embodiment of the present invention. This embodiment exemplifies a part of an analog switch circuit and a wiring structure in the periphery of an image signal line.

[0042]

A switch circuit such as an analog switch requires that an image signal is written in a data line in a short time, and for that reason, high-speed operation is required.

In the conventional high-temperature polysilicon TFT and low-temperature polysilicon TFT, because they are poor in crystallinity in comparison with a monocrystal MOSFET, it was difficult to obtain required high-speed operation when constituting the switch circuit such as the analog switch.

[0043]

A semiconductor region in the thin-film transistor circuit according to the present invention is characterized in that a metal element added region is extended from the semiconductor region by a distance x, to thereby make the grain boundary of the entire semiconductor region more linear.

[0044]

In this embodiment, distance x = 100 μm, interval distance y = 10 μm and width w = 10 μm are set.

In Fig. 3(A), x is substantially identical in length with y and w, but it is merely reduced for construction.

[0045]

Because the semiconductor region according to the present invention is designed such that its crystallization is directed to one orientation in comparison with the conventional high-temperature polysilicon TFT and low-temperature polysilicon TFT, the same high-speed operation as that of the monocrystal MOSFET can be obtained.

[0046]

Fig. 3(A) exemplifies a partial top view of a layout of a data line drive circuit on the substrate in the periphery

of the image signal line.

Fig. 3(C) is a cross-sectional view taken along a line a-a' of Fig. 3(A).

An image signal line V is connected to lead wirings SL1, SL2 and also a data line DL1 through a p-type or n-type semiconductor region.

The image signal line V is designed such that the lead wiring SL1 is electrically connected to the wiring DL1 through a contact hole of the semiconductor with only a necessary image signal.

[0047]

Fig. 3(B) is an equivalent circuit diagram of Fig. 3(A).

In this embodiment, two p-channel type TFTs are connected in series, two n-channel type TFTs are connected in series, and a p-channel type TFT group and an n-channel type TFT group are combined together in parallel and connected as shown in Fig. 3(B).

With this structure, an analog switch circuit is formed which complementarily operates in such a manner that upon turning one transistor group on, the other transistor group is turned off.

[0048]

In this example, two TFTs are connected in series, but, the number of TFTs may be more than two, that is, a large number, or one. It is needless to say that the TFTs are arranged with the size and the number thereof which can withstand the deterioration of the characteristics.

[0049]

The analog switch circuit conducts the operation of switching a high resistance and a low resistance according to a timing which is applied to switch circuit drive gate lines GL1 and GL2 to which a bit signal outputted from a drive timing control section is supplied.

Through the analog switch circuit that complementarily operate as mentioned above, only necessary image signal inputted to the image signal line V is electrically connected to the

data wiring DL1. Thereafter, the signal is transmitted to the respective pixels and displayed on a screen.

[0050]

[Second Embodiment]

A process of manufacturing the structure of the above embodiment will be described hereinafter.

[0051]

First, a silicon oxide film is formed in thickness of 3,000 Å on a quartz substrate 401 as an under film 402. If the surface of the quartz substrate is excellent in smoothness and also satisfactorily cleaned, the under film 402 is not particularly required.

[0052]

Under the existing circumstances, it is a preferable choice to use the quartz substrate as a substrate, however, if it is an insulating substrate that can withstand a heat treatment temperature, the substrate is not limited to quartz.

[0053]

Then, an amorphous silicon film 403 which is a starting film of a crystalline silicon film is formed in thickness of 600 Å through a low pressure CVD method. It is preferable that the thickness of the amorphous silicon film is set to 2,000 Å or less.

[0054]

Thereafter, a silicon oxide film not shown is formed in thickness of 1,500 Å and then patterned to form a mask denoted by reference numeral 404. The mask is opened in a region 405. In the region where an opening 405 is defined, the amorphous silicon film 403 is exposed.

[0055]

The opening 405 is shaped in a slender rectangle which is longitudinal backward and frontward of the drawing. It is proper that a width of the opening 405 is set to 10 μm or more. Also, an end portion of the opening 405 is designed

such that it is apart from an active layer region which will be formed in a post-process by the distance x.

[0056]

Nickel acetate solution containing nickel elements of 10 ppm in weight conversion therein is coated on the surface. Then, spin dry is conducted using a spinner not shown to remove a surplus solution.

[0057]

In the above manner, a state in which the nickel elements exist in a state indicated by a dotted line 406 of Fig. 4(A) is obtained. In this state, the nickel elements are held selectively in contact with a part of the amorphous silicon film on a bottom of the opening 405.

[0058]

The introduction of nickel elements may be conducted through the ion implanting method. In this case, a position at which the nickel elements are introduced can be controlled with higher accuracy in comparison with a case in which a nickel element solution is coated on the surface. Therefore, this is effective particularly in a case where a width of a region into which the nickel elements are introduced is extremely narrow to the degree of several μm or less, or in a case where a shape of the introduced region is complicated.

[0059]

Subsequently, a heat treatment is conducted at 500 to 630 ℃, for example, 600 ℃ for 8 hours in a nitrogen atmosphere containing hydrogen of 3% but little of oxygen. With this process, crystal growth is progressed in parallel to the substrate 401 as indicated by reference numeral 407 in Fig. 4(B).

[0060]

The crystal growth is progressed from a region of the opening 405 into which the nickel elements are introduced (metal element added region) toward a periphery thereof.

[0061]

The surface of the crystalline silicon film which has grown laterally by the crystal growth is very excellent to smoothness in comparison with the conventional low-temperature polysilicon or high-temperature polysilicon. It is presumed that this is caused by the fact that a direction along which the grain boundary extends is substantially unified.

[0062]

The general silicon film which is called polycrystal silicon or polysilicon is 100 Å or more in the roughness of its surface. However, in the case of making crystal laterally grow as in this embodiment, it has been observed that the roughness of its surface is 30 Å or less. Since the roughness of the surface deteriorates the characteristics of the interface between the silicon film and the gate insulating film, it is preferably as small as possible.

[0063]

In heat treatment conditions for the above crystallization, the lateral growth can be conducted over 100 μm or more. Thus, a crystalline silicon film 408 having a laterally grown region is obtained.

[0064]

The heat treatment for crystal growth can be conducted at 450 to 1,100 ℃ (the upper limit is regulated by the heat resistivity of the substrate). If a certain lateral growth distance is ensured, it is preferable that the temperature of the heat treatment is set to 600 ℃ or more. However, an improvement in the crystal growth distance and the crystallinity when the temperature is allowed to rise higher than that temperature does not increase so much.

[0065]

Then, the mask 404 which is formed of the silicon oxide film for selectively introducing the nickel elements is removed. Thus, a state shown in Fig. 4(C) is obtained.

[0066]

In this state, the nickel elements are segregated in the crystalline silicon film 408. In particular, the nickel elements exist with a relatively high concentration in the region where the opening 405 is defined and a top portion of the crystal growth which is indicated by reference numeral 407.

In the regions where the nickel elements are segregated in the film, an orientation of the crystal growth is disordered.

Therefore, in formation of the active layer, it is important to prevent those regions. That is, it is important to prevent the regions in which the nickel elements are segregated from existing in the active layer.

Also, there is designed such that wiring is formed on the region where the opening 405 has been defined.

[0067]

After the state shown in Fig. 4(C) is obtained, a laser beam is applied to the surface. In other words, crystallization may be further promoted by the application of a laser beam. The application of the laser beam has an effect of diffusing a lump of nickel elements which exist in the film so as to be liable to remove the nickel elements later. Even if a laser beam is applied at this stage, the lateral growth is not further progressed.

[0068]

The laser beam can be obtained by using an eximer laser having a wavelength of an ultraviolet region. For example, an KrF eximer layer (248 nm in wavelength) or an XeCl eximer laser (308 nm in wavelength) can be used.

[0069]

Thereafter, a heat treatment is conducted at 950 ℃ under an oxygen atmosphere containing halogen elements therein, for example, an oxygen atmosphere containing HCl of 3 volume % to form a thermal oxide film 409 having a thickness of 200 Å. With the formation of the thermal oxide film, the thickness of silicon film 408 is reduced about 100 Å. In other words,

the thickness of the silicon film becomes about 500 Å.

[0070]

During the above process, with the formation of the thermal oxide film, the silicon elements having an unstable bonding state in the film is used for the formation of the thermal oxide film. Then, defects in the film are reduced, thereby being capable of obtaining higher crystallinity.

[0071]

At the same time, the formation of the thermal oxide film and the gettering of the nickel elements from the film due to the action of chlorine are conducted.

[0072]

It is needless to say that the nickel elements are taken in the thermal oxide film with a relatively high concentration. Then, the nickel elements in the silicon film 408 are relatively reduced.

[0073]

After the formation of the thermal oxide film 409, the thermal oxide film 409 is removed. As a result, a crystalline silicon film 408 having the reduced concentration of the nickel elements contained therein is obtained. The crystalline silicon film thus obtained has a structure in which a crystal structure extends in one direction (this direction is identical with an orientation of crystal growth). In other words, a plurality of slender cylindrical crystals are structured to be aligned in parallel through a plurality of grain boundaries that extend in one direction. Oxygen and chlorine are segregated in the grain boundaries that extend in one direction (this direction is identical with an orientation of crystal growth).

[0074]

Then, patterning is conducted to form a pattern 410 which is formed by a lateral growth region. The island region 410 will be formed into an active layer of the TFT later.

In this situation, the region where the opening 405 is formed is liable to be etched because it contains the nickel

elements more than other regions with the result that the silicon oxide film which is an under film is over-etched as shown in Fig. 4(D).

[0075]

In this process, a pattern is positioned in such a manner that a direction connecting the source region and the drain region is identical with or nearly identical with an orientation of crystal growth. With this process, a direction of moving carriers can be identical with a direction along which crystal lattices continuously extend as a result of which a TFT having a high characteristic can be obtained.

[0076]

Then, after the formation of the pattern 410, a thermal oxide film 511 is formed in thickness of 300 Å (Fig. 5(E)). This thermal oxide film is obtained by conducting a heat treatment of 950 ℃ in an oxygen atmosphere containing HCl of 0.1 to 10 volume%, for example, 3% therein.

[0077]

With the formation of the thermal oxide film 411, the thickness of the pattern (a pattern which is formed into an active layer) 410 becomes 350 Å.

[0078]

In this process, the same effect as the case of forming the thermal oxide film 409 can be obtained. The thermal oxide film 409 is formed into a part of the gate insulating film of the TFT.

[0079]

Thereafter, a silicon oxide film 515 that constitutes the gate insulating film with the thermal oxide film is formed in thickness of 1,000 Å through the plasma CVD method (Fig. 5(F)).

[0080]

Then, an aluminum film for forming a gate electrode is formed in thickness of 4,000 Å through the sputtering method.

Scandium of 0.2 weight% is contained in the aluminum film.

[0081]

The reason why scandium is contained in the aluminum film is to suppress the occurrence of hillock or whisker during a post-process. The hillock and whisker are directed to a needle-shaped or shaped projection which is caused by abnormal growth of aluminum during heating.

[0082]

A material used for forming the gate electrode other than aluminum may be tantalum (Ta), polycrystal silicon which is doped with a large amount of phosphorus (P), silicide of tungsten (WSi), or a lamination layer or mixture of polycrystal silicon which is doped with phosphorus and silicide of tungsten.

[0083]

After the formation of the aluminum film, a fine anodic oxide film not shown is formed. The anodic oxide film is formed in an ethylene glycol solution containing tartaric acid of 3% therein as an electrolyte with aluminum as an anode and platinum as a cathode. In this process, the anodic oxide film having a fine quality is formed in thickness of 100 Å on the aluminum film.

[0084]

The fine anodic oxide film not shown serves to improve an adhesion to a resist mask which will be formed later.

[0085]

The thickness of the anodic oxide film can be controlled according to supply voltage during anodic oxidation.

[0086]

Subsequently, a resist mask 522 is formed. Then, using the resist mask, the aluminum film is patterned into a pattern 518. Thus, a state shown in Fig. 5(G) is obtained.

[0087]

In this stage, anodic oxidation is again conducted. In this situation, oxalic acid aqueous solution of 3% is used as an electrolyte. In the electrolyte, anodic oxidation is

conducted with the aluminum pattern 518 as an anode, to thereby form a porous anodic oxide film 519.

[0088]

In this process, the porous anodic oxide film 519 is selectively formed on the side surfaces of the aluminum pattern because the high-adhesive resist mask 522 exists on the upper side.

[0089]

The porous anodic oxide film can be allowed to grow up to several μm in thickness. In this example, the thickness of the porous anodic oxide film is set to 6,000 Å. The growth distance can be controlled according to an anodic oxidizing time.

[0090]

Then, the resist mask 522 is removed. Thereafter, a fine anodic oxide film is again formed. In other words, anodic oxidation is again conducted in the above-mentioned ethylene glycol solution containing tartaric acid of 3% therein.

[0091]

In this process, an anodic oxide film 520 having a fine quality is formed because the electrolyte enters the porous anodic oxide film 519.

[0092]

The thickness of the fine anodic oxide film 520 is set to 1,000 Å. The thickness of the anodic oxide film can be controlled according to supply voltage.

[0093]

In this situation, the exposed silicon oxide film 515 is etched. At the same time, the thermal oxide film 511 is etched. The etching as used is a dry etching. Then, using a mixed acid where acetic acid, nitric acid and phosphoric acid are mixed together, the porous anodic oxide film 519 is removed. Thus, a state shown in Fig. 5(H) is obtained.

[0094]

After the state shown in Fig. 5(H) is obtained, impurity

ions are implanted. In this process, in order to fabricate an n-channel type thin-film transistor, P (phosphorus) ions are implanted through the plasma doping method.

[0095]

In this process, regions 630 and 634 which are heavy-doped and regions 631 and 633 which are light-doped are formed. This is because the remaining silicon oxide film 515 functions as a semi-transparent mask, and a part of the implanted ions is shielded by the film 515.

[0096]

Then, a laser beam (or an intense light by a lamp) is applied to activate the region into which the impurity ions are implanted. Thus, a source region 630, a channel formation region 632, a drain region 634 and low concentration impurity regions 631, 633 are formed in a self-aligning manner.

[0097]

In this example, what is denoted by reference numeral 633 is a region which is called "an LDD (light dope drain) region" (Fig. 6(I)).

[0098]

In the case where the thickness of the fine anodic oxide film 510 is thickened to 2,000 Å or more, offset gate regions can be formed by this thickness outside of the channel formation region 632.

[0099]

Similarly, in this embodiment, the offset gate region is formed. However, since its dimensions are small such that a contribution of the offset gate region is small, and also the drawings are complicated, the offset gate region is omitted from the drawing.

[0100]

In order to make the anodic oxide film having the fine quality thicker to the degree of 2,000 Å or more, since a supply voltage of 200 V or higher is required, attention must be paid to reproducibility and safety.

[0101]

Subsequently, a silicon oxide film, a silicon nitride film or a lamination film consisting of those films is formed as an interlayer insulating film 640. The interlayer insulating film may consist of a layer which is made of a resin material on a silicon oxide film or a silicon nitride film.

[0102]

Then, contact holes are formed so that a source electrode 641 and a drain electrode 642 are formed. Thus, a thin-film transistor shown in Fig. 6(J) is completed.

[0103]

The TFT according to this embodiment can obtain an extremely high characteristic which could not be obtained by the conventional TFT.

[0104]

For example, an NTFT (n-channel type TFT) as manufactured can obtain a high performance such as the mobility of 200 to 300 (cm^2/Vs) and the S value of 75 to 90 (mV/dec) (V_D = 1 V). A PTFT (p-channel type TFT) as manufactured can obtain a high performance such as the mobility of 120 to 180 (cm^2/Vs) and the S value of 75 to 100 (mV/dec) (V_D = 1 V).

[0105]

In particular, the S value is a wonder excellent value which is 1/2 or less of that in the conventional high-temperature polysilicon TFT and low-temperature polysilicon TFT.

[0106]

The TFT thus manufactured can conduct the operation of 1 GHz in a ring oscillator level and the operation of 100 MHz in the shift register level when a voltage of the drive signal is 3.3 to 5 V.

[0107]

Also, the thin-film transistor employing the crystalline silicon film having the above singular crystal structure is characterized in that the crystal structure makes it hard to exhibit the short channel effect. Also, it is characterized in that since an insulator is used as a substrate, there rises

no problem on the capacity of the substrate, and it is suitable for high-speed operation.

[0108]

The conventional MOS transistor using a monocrystal silicon wafer has a scaling rule. This is that as the dimensions of the transistor are made small in accordance with a predetermined rule, the performance of the transistor is enhanced in accordance with the predetermined rule.

[0109]

However, under the circumstances where the fining of the transistors has been greatly advanced in recent years, it becomes difficult to enhance the performance of the transistor in accordance with that scaling rule.

[0110]

As one example, as a channel length is shortened to suppress the short channel effect, a fine measure such that a portion along the channel is doped with impurities is required, thereby more increasing the difficulty in a manufacture process.

[0111]

However, in the case of using a crystalline silicon film having such a singular crystal structure, a required characteristic can be obtained by the dimensions which are not complied with the above scaling rule.

[0112]

It is presumed that this is caused by items stated below.

(1) A direction along which a columnar crystal extends is identical with a direction of moving carriers in the channel, to thereby suppress the short channel effect.

(2) An insulator is employed for a substrate, to thereby greatly suppress a problem on the capacity.

(3) Since the gate electrode can be made of aluminum, it is advantageous in the high-speed operation.

[0113]

In the item (1), the following can be presumed. That is, each columnar crystal structure is partitioned by an inactive grain boundary. Since the grain boundary portion is high in

energy level, the movement of the carriers is regulated along the crystal extending direction. Also, in the same way, the spread of a depletion layer into the interior of the channel from the source and drain regions is suppressed. It is presumed that this suppresses the short channel effect.

[0114]

Specific examples in which the characteristics are not complied with the above-mentioned scaling rule are stated below.

[0115]

For example, in the case where the thickness of the gate insulating film must be 100 Å in accordance with the conventional scaling rule, if a crystalline silicon film according to the present invention is used, the same characteristics can be obtained with the thickness of the gate insulating film being 300 Å. As a result, the static electricity resistant characteristic can be enhanced.

[0116]

It is understood that this is caused by the above items (1) to (3).

[0117]

Also, not only the thickness of the gate insulating film but also the channel length can provide a predetermined characteristic under the condition more lenient than the conventional scaling rule (condition lower one rank).

[0118]

This is useful in the case where the semiconductor circuit that enables high-speed operation is manufactured over large area at the low costs.

[0119]

[THIRD EMBODYMENT]

This embodiment exhibits an example in which a glass substrate is used as a substrate. In this embodiment, without conducting a process of forming a thermal oxide film that requires processing at a high temperature, instead, a crystalline silicon film where crystal grows in parallel to the substrate is obtained

by application of a laser beam.

[0120]

In other words, there are applied processes such as the selective introduction of nickel elements into the amorphous silicon film, crystal growth in parallel to the substrate by a heat treatment at 600 ℃ for 8 hours, and laser annealing conducted on a crystal growth region.

[0121]

A relation between a position of the region where nickel elements are added and a position at which the active layer is formed is identical with that described with reference to other embodiments.

[0122]

[Fourth Embodiment]

In this embodiment, the structure described in the first to third embodiments is made up of inverted stagger type thin-film transistors. Even if the planner type thin-film transistor in the respective embodiments is replaced by the inverted stagger type thin-film transistor, the same effect can be obtained.

[0123]

As the gate electrode of the inverted stagger type thin-film transistor, to use a material high in heat resistance, for example, polycrystal silicon which is doped with a large amount of phosphorus for the gate electrode is effective in obtaining a high-performance thin-film transistor.

[0124]

[EFFECT OF THE INVENTION]

According to the present invention, since the metal element added region takes a margin of the distance x so as to be longer from the end portion of the semiconductor island region 101 longitudinally, the diffusion state shown in Fig. 2(a) is obtained. Then, using the region where a direction of extending the grain boundary of the semiconductor region 101 is substantially linear (one dimensional), the thin-film transistor can be manufactured.

[0125]

Since the semiconductor region of the present invention is designed such that an orientation of crystallization is linear in comparison with the conventional high-temperature polysilicon TFT and low-temperature polysilicon TFT, the same high-speed operation as that of a monocrystal MOSFET can be obtained.

[0126]

Also, a higher-speed operation can be obtained since a direction of moving the carriers in the semiconductor island region that constitutes the thin-film transistor (a carrier moving direction as a whole) is nearly identical with a direction of the continuity of the crystal structure.

With the structure of the present invention, the characteristics of the transistor can be improved, and a uniform characteristic can be obtained. Further, uniformity of writing an image signal or the like can be kept in the semiconductor device that forms a peripheral circuit.

[0127]

The present invention not only constitutes the peripheral circuit formed on the same substrate as the active matrix circuit in the transmission type or reflection type active matrix liquid-crystal display device, but also is applicable to a display unit employing an EL (electro luminescence) element and a variety of circuits using the thin-film transistors.

[BRIEF DESCRIPTION OF THE FIGURES]

[Figs. 1] a top view schematically showing the present invention and a prior art;

[Figs. 2] diagrams of metal elements diffusion state;

[Figs. 3] diagrams showing a process manufacturing a thin-film transistor of an embodiment;

[Figs. 4] diagrams showing a process manufacturing film transistors of the second embodiment;

[Figs. 5] diagrams showing a process manufacturing film transistors of an embodiment;

[Figs. 6] diagrams showing a process manufacturing an

film transistors of an embodiment;

[DESCRIPTION OF A MARK]

101 semiconductor region
102 source line
103 gate line
104 drain line
105 metal element added region of this invention
106 metal element added region of prior art
305 metal element added region
401 quartz substrate
402 under film
403 amorphous silicon film
404 mask formed of silicon oxide film
405 opening region of mask (metal element added region)
406 Ni elements held in contact with substrate
407 crystal growth direction
408 crystalline silicon film
409 thermal oxide film
410 pattern region
511 thermal oxide film
515 silicon oxide film (gate insulating film)
518 aluminum film
519 porous anodic oxide film
520 fine quality oxide film
522 resist mask
630 source region
631 low concentration impurity region
632 channel region
633 low concentration impurity region (LDD region)
634 drain region
640 interlayer insulating film
641 source electrode
642 drain electrode

[NAME OF DOCUMENT] Document of abstract

[ABSTRACT]

[PURPOSE]

To provide a method of manufacturing a thin-film transistor circuit that requires high-speed operation (in general, the operation speed of several tens MHz or more)

[METHOD TO ATTAIN THE PURPOSE]

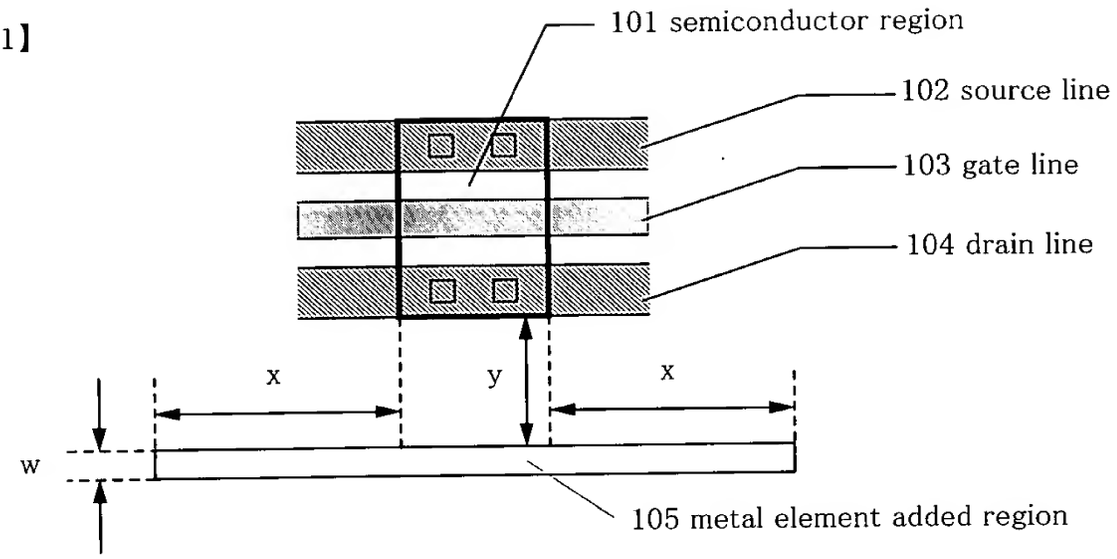
In a circuit having at least one thin-film transistor formed on an insulating substrate, the metal element added region 105 is disposed apart from a semiconductor island region 101 that forms said thin-film transistor by a distance y, has a width w, and extends longitudinally over an end portion of the semiconductor island region 101 by a distance x.

[SELECTED FIGURE] Figs. 1

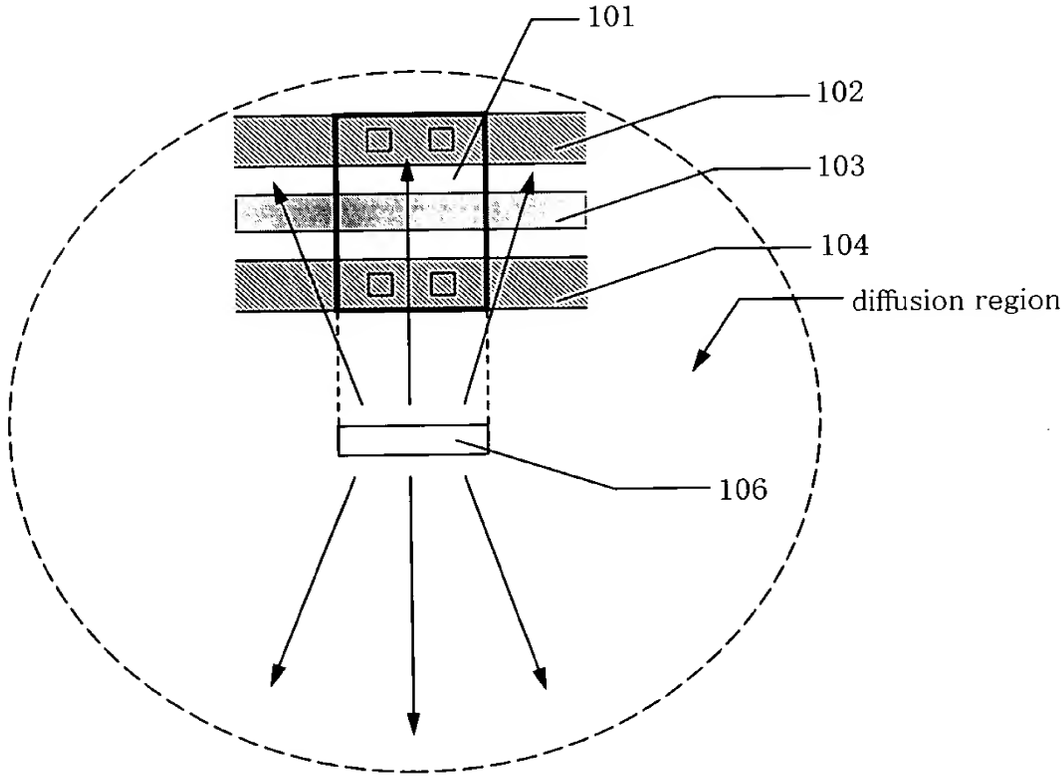
【Reference Number】 P003521-04

【Document】 Figures

【Figs. 1】



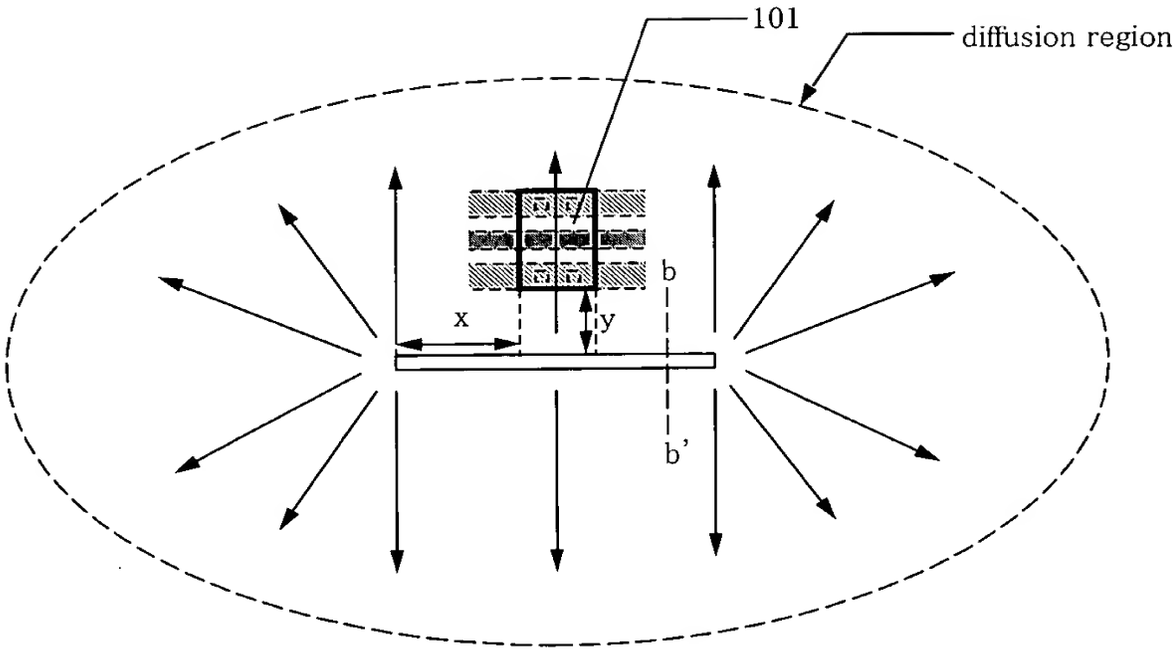
(a) top view showing present invention



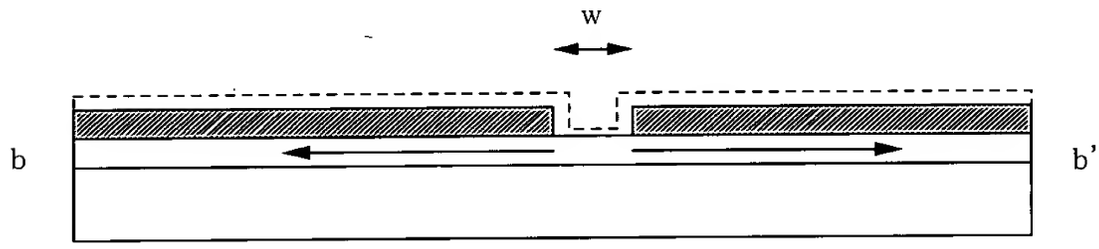
(b) prior art

【Reference Number】 P003521-04

【Figs. 2】



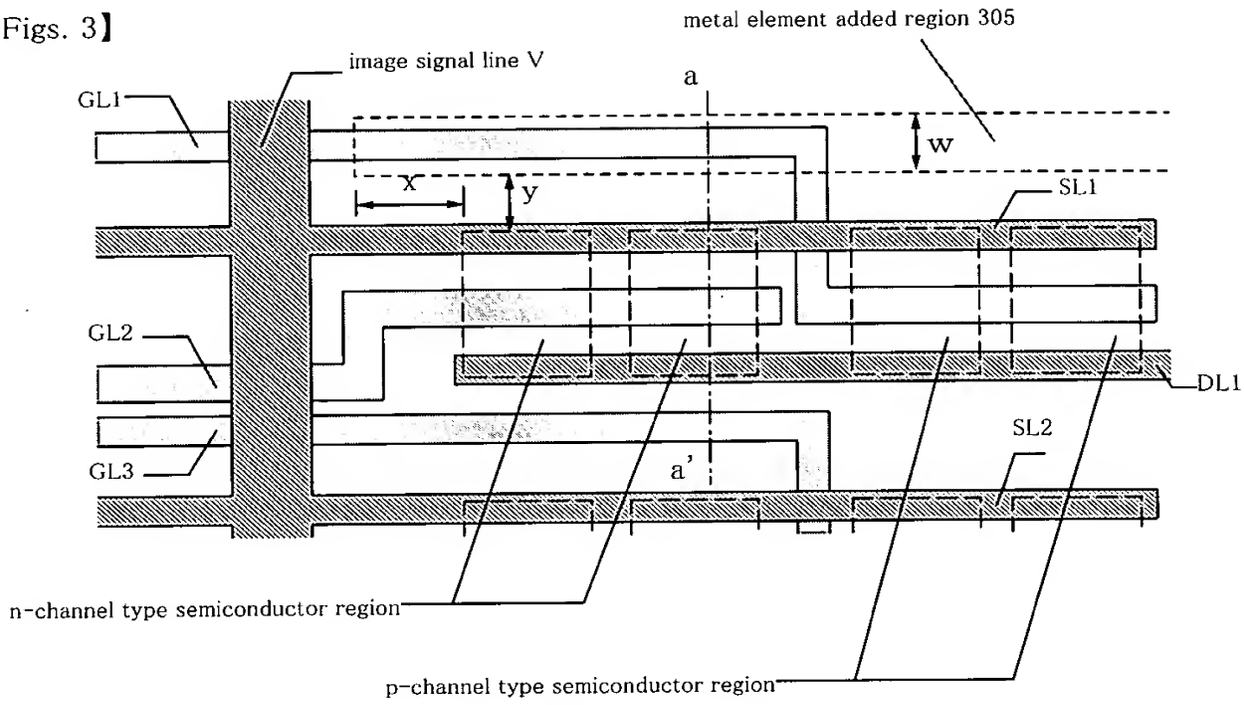
(a) top view of showing diffusion state



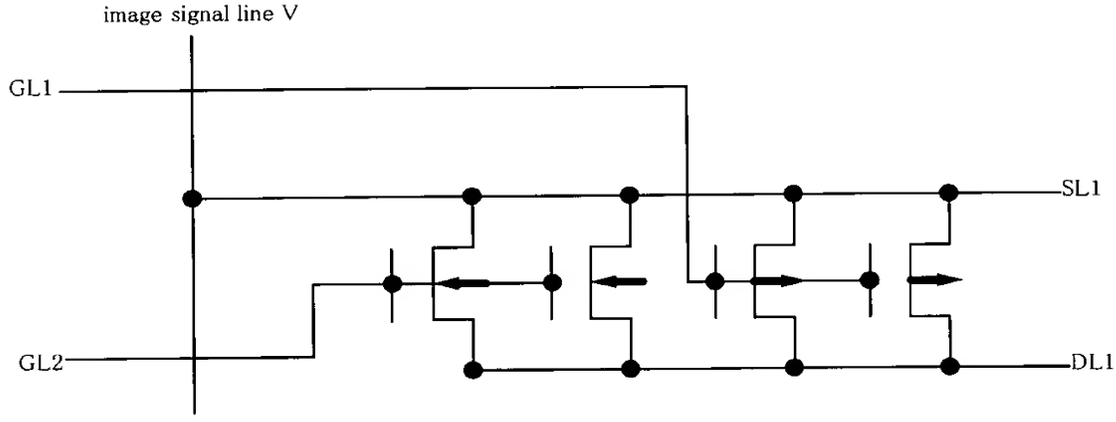
(b) b-b' cross section view

【Reference Number】 P003521-04

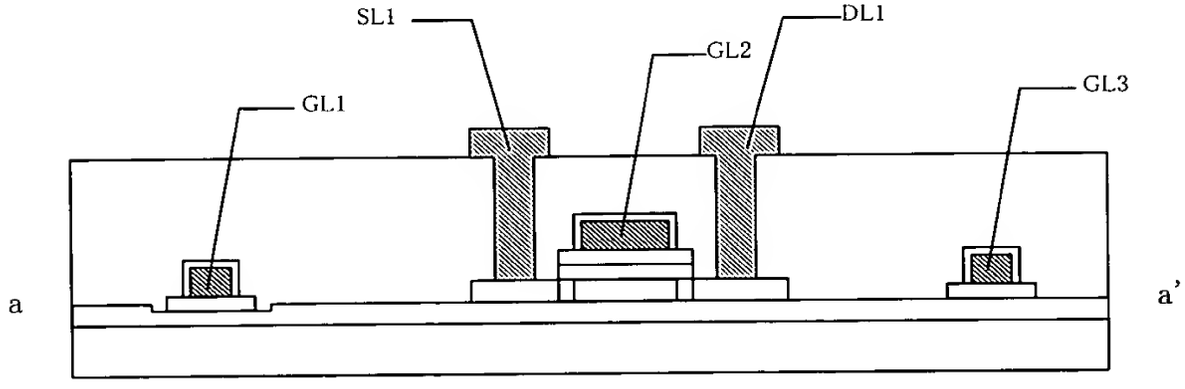
【Figs. 3】



(A) top view



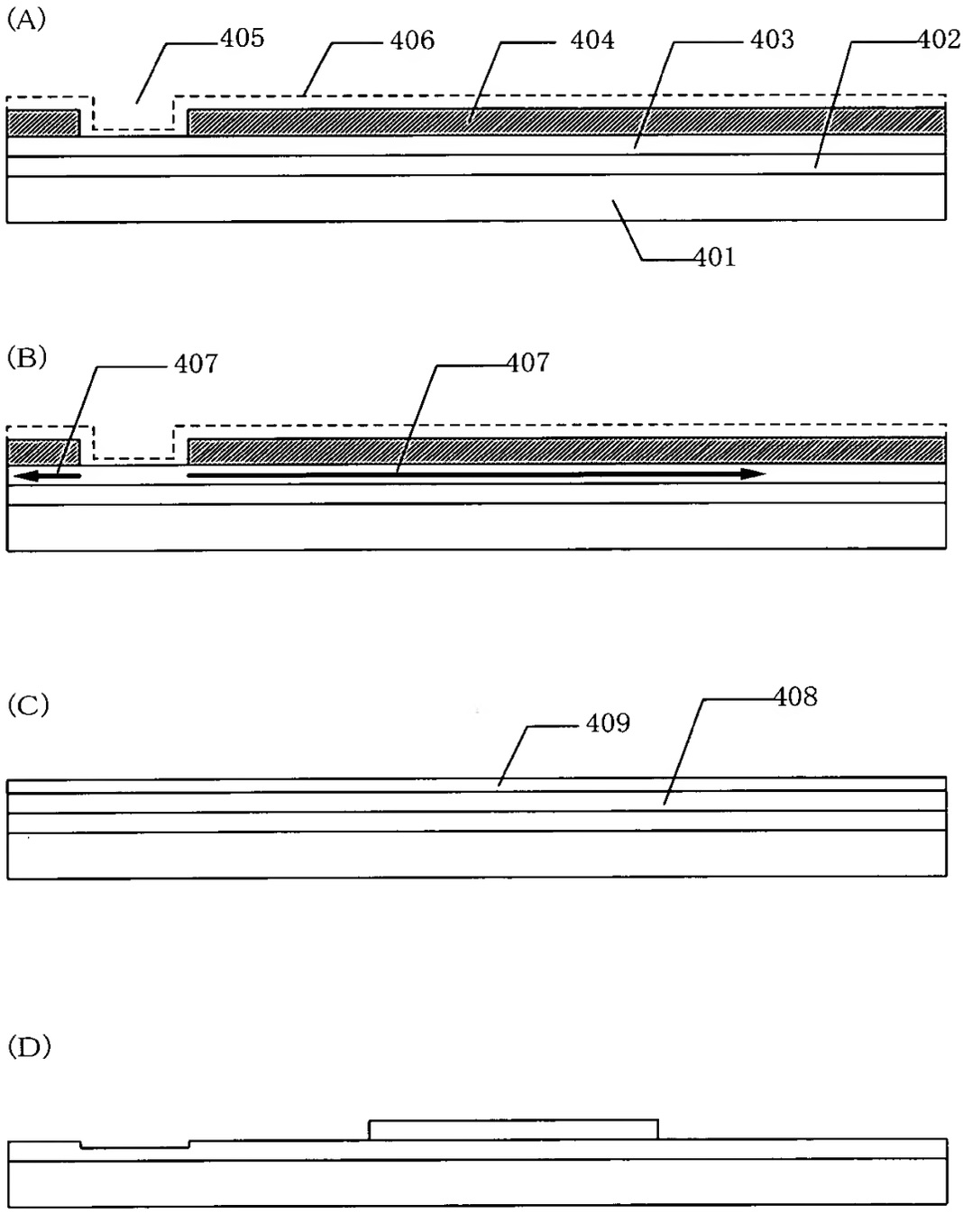
(B) equivalent circuit



(C) a-a' cross section view

【Reference Number】 P003521-04

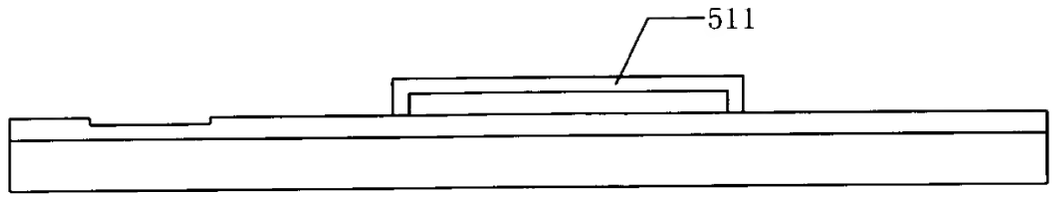
【Figs. 4】



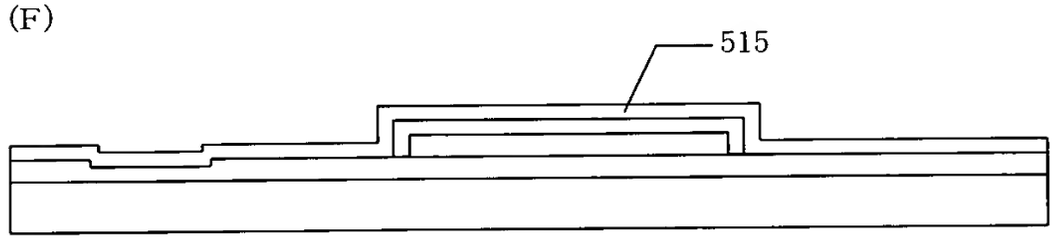
【Reference Number】 P003521-04

【Figs. 5】

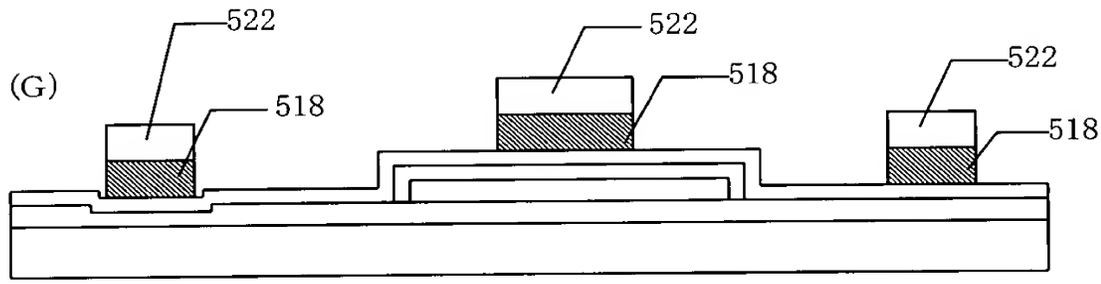
(E)



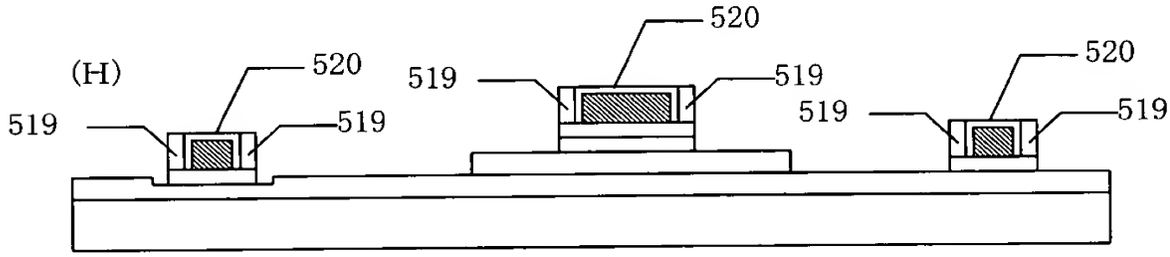
(F)



(G)



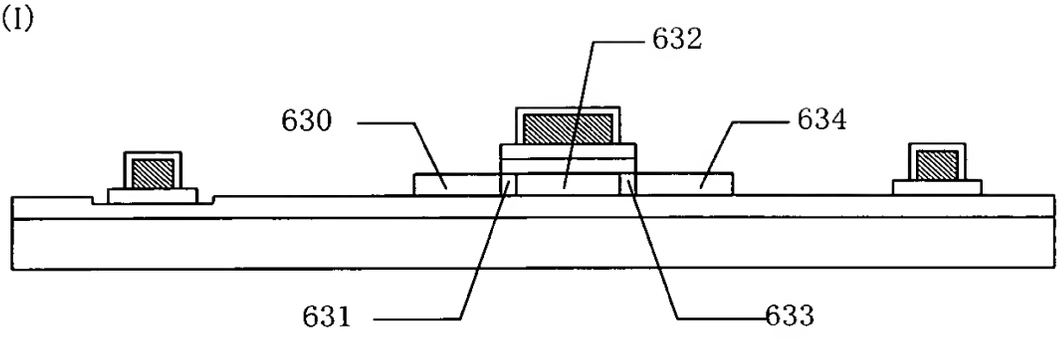
(H)



【Reference Number】 P003521-04

【Figs. 6】

(I)



(J)